REMARKS

Reconsideration of the rejections contained in the Office Action is respectfully requested. By this amendment claims 3-4, 6-7, 9, 11, and 16 have been canceled without prejudice or disclaimer, and claims 1-2, 5, 8, 10, 12, and 15 have been amended. Currently, claims 1-2, 5, 8, 10, and 12-15 are pending in this application.

Rejection under 35 USC 112

Claims 8-16 were rejected under 35 USC 112, second paragraph, as indefinite. Applicants have amended the claims to overcome this rejection and respectfully request that it be withdrawn.

Rejection under 35 USC 102 and 103

Claims 12-14 were rejected under 35 USC 102 as anticipated by Wilford (U.S. Patent No. 6,968,392). Claims 1, 3-9 and 15-16 were rejected under 35 USC 103 as unpatentable over Wilford in view of Dugatkin (U.S. Patent Application Publication No. 2004/0236866). Claims 2, 10, and 11 were rejected under 35 USC 103 over Wilford in view of Donati (U.S. Patent No. 7,007,099). These rejections are respectfully traversed in view of the amendments to the claims and the following arguments.

This application relates to a method for selectively reading counter information in a network element. As described by applicants in the background section (see e.g. page 1, lines 19-32) a network element may need to maintain many statistics on various aspects of the traffic that is passing through the network element. Each of these statistics will have a separate counter. Since counters are limited in size by the hardware that is used to implement the network element, the counters need to be read periodically, such as once every .01 second. Reading a large number of counters 100 times per second is a large amount of overhead for the network element processor.

Applicants proposed to count statistics using counters and, when a particular threshold unrelated to time was reached, such as the counter was half full, the counter would set a bit or other type of flag to cause it to be read. (See Specification page 12, line 12 to page 13, line 14). In the specification, applicants state that a "ripeness indicator" "is used to signal to the network device when one or more counters has met or exceeded a predetermined value." Specification at

page 2, lines 15-16. Thus, the term "ripeness indicator" specifies when a counter has met or exceeded a predetermined value and relates to the content of the counter itself.

Applicants proposed to use an array of direct addressable words, each of which contains a number of ripeness indicators (see e.g. Specification at page 12, lines 3-14). For example, each of the words 92 may include 32 bits 94. Where the CPU is capable of handling larger direct addressable words such as 64 bit words, then other sized words may be used and the claims are not limited to 32 bit words.

When a statistics counter reaches a threshold value, a bit within this array is set indicating that the counter (or counters) associated with that statistic are ready to be harvested. (Specification at page 12, lines 14-16). When the statistics co-processor is ready to read counters, it will read the array of ripeness indicators to determine which accounts contain counters that are ready to be harvested. From the array of ripeness indicators the statistics co-processor learns what subset of counters should be read, and then only those counters are read.

Wilford teaches a system in which comparators are used to determine when particular adders have exceeded threshold values. (Wilford at col. 6, lines 16-34). Whenever a comparator exceeds its threshold value, a FIFO control unit 308 operates to send an interrupt signal to CPU 302. (Wilford at Col. 7, lines 60-67; Col. 8, lines 16-18). This enables the CPU to poll adders associated with high traffic connections more frequently than other adders (Wilford at Col. 8, lines 28-32).

Applicants have amended the claims to focus on an embodiment where an array of ripeness indictors is used to notify the statistics co-processor which of the accounts should be harvested. This type of array is not taught or suggested by Wilford. Likewise, although the Examiner indicated that Dugatkin teaches the use of threshold values, Dugatkin does not teach or suggest the use of an array of ripeness indicators to signal to the statistics co-processor which of the counters should be processed, and likewise does not teach or suggest that the statistics co-processor should only harvest statistics from those counters identified in the ripeness indicator array.

Claim 10 previously recited the use of an array of ripeness indicators. In rejecting this claim, the Examiner cited Donati (U.S. Patent No. 7,007,099). In particular, the Examiner indicated that Donati taught the use of an array of ripeness indicators at Col. 63, lines 54-67.

To understand this portion of Donati, applicants would first like to direct the Examiner's attention to Col. 29, lines 12-24. In this portion, Donati explains that garbage on one of the channels can use up all of the RVC message buffer pointers. Accordingly, Donati proposes to use three programmable error threshold registers to monitor three particular types of errors – short frame, long frame, and CRC errors. Whenever a short frame, long frame, or CRC error occurs, the corresponding count is incremented. The counters are reset every 10 msec. If one of the counters exceeds its respective threshold, the error bit will be set.

The error bits are set in an error source register, but do not halt operation of the device. The portion of Donati cited by the Examiner explains the error source register in greater detail. In particular, Fig. 53 of Donati shows the Error Source Register (See Donati at Col. 62, lines 51-66, Col. 63, and Col. 64, lines 1-42). The Error Source Register summarizes all of the detected errors. (Donati at Col. 62, line 52). The several bits that are set in this register do not instruct the processor that statistics are to be collected from particular counters, but rather provide an indication of the type of error that occurred.

Accordingly, the cited references alone and in combination fail to teach or suggest that an array of ripeness indicators should be maintained, and that the array of ripeness indicators should be read first to determine a subset of counters that should be processed. In view of the claim amendments, applicants therefore respectfully request that the rejection under 35 USC 103 be withdrawn.

Conclusion

Applicants respectfully submit that the application is in condition for allowance and an action to this effect is respectfully requested. If there are any questions or concerns regarding the amendments or these remarks, the Examiner is requested to telephone the undersigned at the telephone number listed below.

Extension of Time

Applicant requests a one month extension of time to respond to the Office Action, the fee for which is being paid concurrently herewith. If any additional fees are due in connection with this filing, the Commissioner is hereby authorized to charge payment of the fees associated with

this communication or credit any overpayment to Deposit Account No. 141315 (Ref. 16128BAUS01U).

Respectfully Submitted

Dated: October 26, 2009

/John C. Gorecki/ .
John C. Gorecki, Reg. No. 38,471

Anderson Gorecki & Manaras LLP
P.O. Box 553
Carlisle, MA 01741
Tel: (978) 264-4001
Fax: (978) 264-9119